WHAT IS CLAIMED IS:

semiconductor substrate.

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1	1.	A method of fabricating a multi-chip module, comprising:
2		partitioning an integrated circuit design to include a first circuit segment and a second
3		circuit segment, wherein functionality associated the first circuit segment and
4		functionality associated with the second circuit segment jointly enable
5		functionality of the integrated circuit design;
6		fabricating a first semiconductor device capable of enabling said functionality associated
7		with the first circuit segment and including an array of first device interconnect
8		pads;
.9		fabricating a second semiconductor device capable of enabling said functionality
T 0		associated with the second circuit segment and including an array of second
11		device interconnect pads; and
12		facilitating direct interconnection between each one of said first device interconnect pads
11 12 13		and a corresponding one of said second device interconnect pads.
<u>-</u> 1	2.	The method of claim 1 wherein partitioning the integrated circuit design to include a first
2		circuit segment and a second circuit segment includes defining a first functional block of
		the integrated circuit design and a second functional block of the integrated circuit design
1	3.	The method of claim 2 wherein defining the first functional block and the second
2		functional block includes defining a memory functional block and a logic functional
3		block, respectively.
1	4.	The method of claim 1 wherein partitioning the integrated circuit design to include a first
2		circuit segment and a second circuit segment includes partitioning the integrated circuit
3		design such that the first circuit segment is associated with a first type of semiconductor

substrate and the second circuit segment is associated with a second type of

circuit segment and a second circuit segment includes partitioning the design such that the first circuit segment is associated with a first semi fabrication process and the second circuit segment is associated with a semiconductor fabrication process. The method of claim 1 wherein: fabricating the first semiconductor device includes fabricating the first	gn to include a first
fabrication process and the second circuit segment is associated with a semiconductor fabrication process. The method of claim 1 wherein: fabricating the first semiconductor device includes fabricating the first	integrated circuit
 semiconductor fabrication process. 6. The method of claim 1 wherein: fabricating the first semiconductor device includes fabricating the first 	conductor
 1 6. The method of claim 1 wherein: 2 fabricating the first semiconductor device includes fabricating the first 	second
fabricating the first semiconductor device includes fabricating the first	
device for heir a south a for which for the constituted or	semiconductor
device for being capable of enabling functionality associated w	rith a first
functional block of the integrated circuit design; and	
fabricating the second semiconductor device includes fabricating the s	econd
semiconductor device for being capable of enabling functional	ity associated with
functional block of the integrated circuit design; and fabricating the second semiconductor device includes fabricating the s semiconductor device for being capable of enabling functional a second functional block of the integrated circuit design. 7. The method of claim 1 wherein:	
1 7. The method of claim 1 wherein:	
fabricating the first semiconductor device includes fabricating a DRAI	M device; and
fabricating the first semiconductor device includes fabricating a DRAI fabricating the second semiconductor device includes fabricating a log	ic device.
1 8. The method of claim 1 wherein:	
2 fabricating the first semiconductor device includes fabricating the first	semiconductor
device from a first type of semiconductor substrate; and	•
4 fabricating the second semiconductor device includes fabricating the s	econd
semiconductor device from a second type of semiconductor sul	bstrate.

1	9.	The method of claim T wherein.
2		fabricating the first semiconductor device includes fabricating the first semiconductor
3		device using a first semiconductor fabrication process; and
4		fabricating the second semiconductor device includes fabricating the second
5		semiconductor device using a second semiconductor fabrication process.

- The method of claim 1 wherein facilitating direct interconnection between each one of said first device interconnect pads and a corresponding one of said second device interconnect pads includes forming a solder-type interconnect between each one of said first device interconnect pads and the corresponding one of said second device interconnect pads.
 - 11. The method of claim 10 wherein forming the solder-type interconnect includes forming a solder bump interconnect.
 - 12. The method of claim 10 wherein forming the solder-type interconnect includes forming a solderball ball interconnect.

1	13.	A method of fabricating a multi-chip module, comprising:
2		partitioning an integrated circuit design to include a first functional block and a second
3		functional block, wherein functionality associated the first functional block and
4		functionality associated with the second functional block jointly enable
5		functionality of the integrated circuit design;
6		fabricating a first semiconductor device capable of enabling said functionality associated
7		with the first functional block and including an array of first device interconnect
8		pads;
9		fabricating a second semiconductor device capable of enabling said functionality
10		associated with the second functional block and including an array of second
Ü		device interconnect pads; and
12		facilitating a solder-type interconnect directly between each one of said first device
13		interconnect pads and a corresponding one of said second device interconnect
14		pads.
	14.	The method of claim 13 wherein partitioning the integrated circuit design to include the
2		first functional block and the second functional block includes defining a memory
		functional block and a logic functional block, respectively.
1	15.	The method of claim 13 wherein partitioning the integrated circuit design to include a
2		first functional block and a second functional block includes partitioning the integrated
3		circuit design such that the first functional block is associated with a first type of
4		semiconductor substrate and the second functional block is associated with a second type
5		of semiconductor substrate.

- 1 16. The method of claim 13 wherein partitioning the integrated circuit design to include a
 2 first circuit functional block and a second functional block includes partitioning the
 3 integrated circuit design such that the first functional block is associated with a first
 4 semiconductor fabrication process and the second functional block is associated with a
 5 second semiconductor fabrication process.
- 1 17. The method of claim 13 wherein forming the solder-type interconnect includes forming a solder bump interconnect.
 - 18. The method of claim 13 wherein forming the solder-type interconnect includes forming a solder ball interconnect.

ı	19.	A muni-cinp module, comprising.
2		a first semiconductor device capable of enabling functionality associated with a first
3		circuit segment of an integrated circuit design and including an array of first
4		device interconnect pads;
5		a second semiconductor device capable of enabling functionality associated with a second
6		circuit segment of the integrated circuit design and including an array of second
7		device interconnect pads; and
8		a plurality of device interconnect members, each one of said device interconnect members
9		being electrically connected directly between one of said first device interconnect
10		pads and a corresponding one of said second device interconnect pads.
	20.	The multi-chip module of claim 19 wherein:
	20.	the first semiconductor device includes is capable of enabling functionality associated
j'Z al		with a first functional block of the integrated circuit design; and
<u>ک</u>		
4		the second semiconductor device is capable of enabling functionality associated with a
5		second functional block of the integrated circuit design.
	21.	The multi-chip module of claim 19 wherein:
2		the first semiconductor device is a DRAM device; and
3		the second semiconductor device is a logic device.
1	22.	The multi-chip module of claim 19 wherein:
2		the first semiconductor device is made from a first type of semiconductor substrate; and
3		the second semiconductor device is made from a second type of semiconductor substrate.
1	23.	The multi-chip module of claim 19 wherein each one of said device interconnect
2		members is a solder-type interconnect member.
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- 1 24. The multi-chip module of claim 23 wherein the solder-type interconnect member is a solder bump.
- 1 25. The multi-chip module of claim 23 wherein the solder-type interconnect member is a
- solder ball.

1	26.	A multi-chip module, comprising:
2		a first semiconductor device capable of enabling functionality associated with a first
3		functional block of an integrated circuit design and including an array of first
4		device interconnect members;
5		a second semiconductor device capable of enabling functionality associated with a second
6		functional block of the integrated circuit design and including an array of second
7		device interconnect members; and
8		a plurality of solder-type interconnect members, each one of said solder-type interconnect
9		members being electrically connected directly between one of said first device
10		interconnect members and a corresponding one of said second device interconnect
n		members.
	27.	The multi-chip module of claim 26 wherein:
	21.	the first semiconductor device is a DRAM device; and
3 ==		the second semiconductor device is a logic device.
	28.	The multi-chip module of claim 26 wherein:
2		the first semiconductor device is made from a first type of semiconductor substrate; and
3		the second semiconductor device is made from a second type of semiconductor substrate.
1	29.	The multi-chip module of claim 26 wherein the solder-type interconnect member is a
2	2).	solder bump.
2		solder outlip.
1	30.	The multi-chip module of claim 26 wherein the solder-type interconnect member is a
2		solder ball.

1	31.	An electronic package, comprising:
2		an interposer circuit including a dielectric substrate and an array of routing elements
3		attached to the dielectric substrate;
4		a first semiconductor device capable of enabling functionality associated with a first
5		circuit segment of an integrated circuit design and including an array of first
6		device interconnect pads;
7		a second semiconductor device capable of enabling functionality associated with a second
8		circuit segment of the integrated circuit design, including an array of second
9		device interconnect pads and including a set of package-level interconnect pads;
10		a plurality of device interconnect members, each one of said device interconnect members
ij		being electrically connected directly between one of the said first device
2		interconnect pads and a corresponding one of said second device interconnect
H		pads; and
4		a plurality of package-level interconnect members, each one of said package-level
1 5		interconnect members being electrically connected between one of the said
16		package-level interconnect pads of the second semiconductor device and a
7		corresponding one of said routing elements of the interposer circuit.
	32.	The electronic package of claim 31 wherein:
2	<i>J</i> 2.	the first semiconductor device includes is capable of enabling functionality associated
3		with a first functional block of the integrated circuit design; and
4		the second semiconductor device is capable of enabling functionality associated with a
5		second functional block of the integrated circuit design.
3		second functional block of the integrated enough design.
1	33.	The electronic package of claim 31 wherein:
2	JJ.	the first semiconductor device is a DRAM device; and
2		the second semiconductor device is a logic device

The electronic package of claim 31 wherein:

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1	40.	An ejectronic package, comprising:
2		an interposer circuit including a dielectric substrate and an array of routing elements
3		attached to the dielectric substrate;
4		a first semiconductor device capable of enabling functionality associated with a first
5		functional block of an integrated circuit design and including an array of first
6		device interconnect members;
7		a second semiconductor device capable of enabling functionality associated with a second
8		functional block of the integrated circuit design and including an array of second
9		device interconnect members; and
10		a plurality of solder-type interconnect members, each one of said solder-type interconnect
H		members being electrically connected directly between one of the said first device
12		interconnect members and a corresponding one of said second device interconnect
13		members; and
1 4		a plurality of package-level interconnect members, each one of said package-level
15		interconnect members being electrically connected between one of the said
16		package-level interconnect pads of the second semiconductor device and a
17		corresponding one of said routing elements of the interposer circuit.
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i 1	41.	The electronic package of claim 40 wherein:
2	71.	the first semiconductor device is a DRAM device; and
3		the second semiconductor device is a logic device.
5		the second semiconductor device is a regic device.
1	42.	The electronic package of claim 40 wherein:
2		the first semiconductor device is made from a first type of semiconductor substrate; and
3		the second semiconductor device is made from a second type of semiconductor substrate.
. 1	43.	The electronic package of claim 40 wherein the solder-type interconnect member is a
2		solder bump.

- 1 44. The electronic package of claim 40 wherein the solder-type interconnect member is a solder ball.
- 1 45. The electronic package of claim 40 wherein:
 2 the interposer circuit is a flip-chip interposer circuit; and
 3 each one of said package-level interconnect members is a solder-type interconnect
 4 member.
 - 46. The electronic package of claim 40 wherein:
 the interposer circuit is a wire-bond interposer circuit; and
 each one of said package-level interconnect members is a conductive wire.